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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 10/626,507
Filing Date: July 24, 2003
Appellant(s): HO ET AL.

Michael D. Wiggins
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed March 06, 2008 appealing from the Office action mailed May 02, 2007.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The following are the related appeals, interferences, and judicial proceedings known to the examiner which may be related to, directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal:

Application No. 10/646,289.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

6,601,126	Zaidi et al.	7-2003
5,699,551	Taylor et al.	12-1997
7,133,972	Jeddeloh	11-2006
6,928,525	Ebner et al.	8-2005
6,725,334	Barroso et al.	4-2004
4,008,460	Bryant et al.	2-1977

The Cache Memory Book, second edition by Jim Handy, pub. 1998, pp 14-17, 42-47, 54-55 and 57.

Adapting Cache Line Size to Application Behavior, by Veidenbaum et al. copyright ACM 1999, pp.145-154

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-5, 11,13-15, 20, 44-48, 50, 52-54, 79-83, 89, 91-92, and 97 are rejected under 35 U.S.C. 103(a) as being unpatentable in view of Zaidi et al. (US 6,601,126 B1) (Zaidi herein after), Jim Handy (The Cache Memory Book, second edition, published 1998) (Jim herein after), Taylor et al. (5,699,551) (Taylor herein after) and Jeddeloh (US 7,133,972).

As per claims 1, 44, 50 and 79, Zaidi teaches a cache control system (fig. 1) that controls data flow between a line cache (fig, 1, item 126), a first central processing unit (CPU) (fig. 1, item 110) and first and second memory devices (fig. 1, items 106 and 108), comprising:

a first line cache interface that is associated with the first CPU (taught as cache and channel controller interface the CPU bus, column 4, lines 39-41), that receives a first program read request from CPU and that generates a first address from said first program read request (column 23, lines 30-32);

a first memory interface that communicate with first memory device and second memory interface that communicates with the second memory device (figs. 21-23, two

memory devices, flash and SDRAM are connected to memory bus through MAC, which teaches first and second interfaces connected to first and second memory devices);

a cache that receives address that includes memory select portion; and a switch that selectively connects said line cache to one of said first and second memory interfaces (fig. 1, item 126 is a cache and even though it is explicitly not taught, when CPUs are provided with cache, CPUs initially try to access data from cache, thus cache receives address, column 23, lines 31-34 and lines 41-45, taught as CPUs supply a request and an address, the address includes both the port, device or memory bank address [memory select portion] and the requested memory location address. Referring figs. 20-23, col. 23 lines 22-29, "switched channel memory controller" allows multiple DMA (and processors) to simultaneously communicate with multiple output channels. Also, col. 23, lines 40-45, suggests that CPU bus can be connected to an external flash memory through one channel and SDRAM through another channel. These statements clearly state that there is separate and selective communication interfaces between the connections, figs. 21, 22 and 23 shows separate lines are connected to the memory interfaces). **(switch providing separate/distinct interfaces are known in the art, because a separate and independent interface avoids bus or memory bank conflict and hence increases the speed of the system [motivation to use switch], see Jeddeloh US 7,133,972, fig. 3, col. 4, lines 30-64, presented as an evidentiary reference).**

Zaidi explicitly fails to teach line cache receiving first address and comparing address to stored addresses and if match occurs it returns data to CPU, and retrieves data from one of the first and second memories if miss occurs, but a system with processor and cache memory is well known to one of ordinary skill in the art at the time

of invention, and when CPU issues read request in such a system, cache compares the address with the stored addresses and returns the data to CPU and if miss occurs it retrieves data from higher latency storages (Jim, page 42-43, section 2.1.3) (also applicant's admitted prior art in the background of the invention section).

Zaidi teaches sending first address with bank (memory) select portion and memory location address (Zaidi, col. 23, lines 31-34) but fails to teach sending a second address based on first address. Taylor teaches computer systems using physical cache, which requires address translation occurring before the cache access (cache receiving translated/second address based on first address) (Taylor, column 1, lines 26-40). It would have been obvious to one having ordinary skill in the art at the time of the invention to utilize physical cache as taught by Taylor in the system of Zaidi and Jim because virtual memory provides protection; large address space and physical cache memories are simpler to build (Taylor, column 1, lines 26-40).

Zaidi, Jim and Taylor explicitly fail to teach the limitation "wherein said switch includes a plurality of selectors that each receives the second address and each select between first and second sets of signals relating to the first and second memory devices, respectively based on the second address". However, Zaidi teaches CPUs connect to either SRAM or flash memory through switched channel memory controller as explained above, and the selection of respective signals are inherent in the system of Zaidi, because it is well known at the time of the invention to one having ordinary skill in the art that the signals (such as clock and request and acknowledgement etc.) are required for proper communication to be occur between the processor and cache or

between cache and lower level storage systems (**see Jeddeloh, col. 4, lines 8-29, "the memory hub (switch) includes a processor interface 150 that is coupled to the processor 104 through a plurality of bus and signal lines, as is well known in the art". Jeddeloh, col. 4, lines 56-67, "for example, the switch 160 may be a cross-bar switch that can simultaneously couple at the processor interface and the memory interfaces 170a-c to each other. The switch can also be a set of multiplexers (plurality of selectors)").**

As per claims 2-3, 45-46 and 80-81, Zaidi teaches that the first memory device is RAM (fig. 1, item 108).

As per claims 4, 47 and 82, Zaidi teaches the second memory device is flash memory (fig. 1, item 106).

As per claim 5, 48 and 83, Zaidi teaches the first CPU is an advanced risc machine (ARM) processor (column 5, lines 35-36).

As per claims 11 and 89, Zaidi teaches a cache memory as per claim 1 and memories are used for storing data. Zaidi fails to teach cache with a Content Addressable Memory (CAM). Jim teaches a cache memory with CAM, which stores addresses associated with data stored in the cache memory (page 14, sec. 1.5, and page 15, fig. 1.7). Jim teaches determining when hit and miss occurs and retrieves data from higher latency memories (first and second memories) when miss occurs (Jim, pages 42-43, sec. 2.1.3 and pages 46-47, fig. 2.4). Thus Jim inherently teaches cache state machine.

It would have been obvious to one having ordinary skill in the art at the time of invention have used Zaidi's dual processor system and modified to use the cache with CAM as taught by Jim because CAM permits content of memory to be searched and

matched instead of having to specify a memory location in order to retrieve data from memory (Jim, page 14, sec. 1.5). This allows data to be stored at any location in a cache (Jim, page 16, paragraph 3)

As per claims 13-14, 52-53 and 91-92, Jim teaches a cache replacement algorithm Least Used Page, which replaces least used page with data retrieved form the first or second memory when miss occurs (page 57, paragraph 2, page 61, pars. 3-4). Thus Jim inherently teaches least used page device.

As per claims 15 and 54 Jim teaches that state transitions of cache state machine are based, in part on at least one internal state of the CPU (page 42, paragraph 2 and 3 and sec. 2.1.3)

As per claims 20 and 97, Jim teaches that cache can have many ways of implementations depending upon the address bits used in the system (page 54, paragraphs 2 and 3). Thus Jim inherently teaches cache with 4 pages of 8 x 32.

3. Claims 16-18, 55-57 and 93-95 are rejected under **35 U.S.C. 103(a)** as being unpatentable in view of Zaidi, Jim Handy, Taylor and Jeddeloh and in further view of Bryant et al. (4,008,460).

Claims 16-18 are similar in scope with combination of claims 1, 11, 13 and 14. Zaidi, Jim Handy, Taylor and Jeddeloh teach all the limitations of claim 16, including identifying first least used page and replacing first least used page in case of cache miss (limitation of claim 17) but fail to teach identifying first and second used page and

replacing second least used page (claim 18). Bryant teaches identifying first and second least used page and replacing second least used page (Bryant, col. 3, lines 52-57).

It would have been obvious to one having ordinary skill in the art at the time of the invention to utilized first and second least used page replacement method as taught by Bryant in the system of Zaidi, Jim Handy, Taylor and Jeddeloh to avoid wrap-around delay associated with LRU policy and increase system performance (Bryant, col. 2, lines 7-16, lines 43-46).

Claims 55-57 and 93-95 are rejected under same rationales as applied to claims 1, 11, 13-14 and 16-17.

4. Claims 6, 21-24, 28, 49, 59-63, 84, 98-101 and 105 are rejected under **35 U.S.C. 103(a)** as being unpatentable over Zaidi, Jim Handy, Taylor and Jeddeloh as applied to claims 1-5, 11, 13-15, 44-48 and 79-83 above, and further in view of Barroso et al. (US 6,725,334 B2).

As per claims 6, 49 and 84, Zaidi and Jim teach a dual processor system with two caches (fig. 2, items 202 and 214, first and second processors, and items 208 and 224, two caches). Zaidi, Jim and Taylor inherently teach cache interface with first and second CPUs and both generates read requests and hence first and second address as taught in claim 1. Zaidi teaches system with two second level caches for two processors but fails to teach cache arbitration device which communicates with first and second cache interfaces and resolves cache access conflicts between first and second CPUs. Barroso teaches a second level cache with switch (fig. 1, item 130 and 120), which

provides interfaces with first and second CPU and arbitrates between first and second CPU (column 4, lines 10-21) **(switch providing separate/distinct interfaces are known in the art, because a separate and independent interface avoids bus or memory bank conflict and hence increases the speed of the system, see Jeddeloh US 7,133,972, fig. 3, col. 4, lines 30-64, presented as an evidentiary reference).**

It would have been obvious to one having ordinary skill in the art at the time of invention would have modified the multiple cache with multiple processor system of Zaidi and used one cache with switch as taught by Barroso to reduce the cost and the waste of the cache capacity (column 1, lines 45-65).

Claims 21-24, 59-63, 84, 98-101 and 105 are similar in scope with combination of claims 1-6, 11, 13-15 and hence rejected under same rationales as applied to claims 1-6, 11 and 13-15 above.

5. Claims 7-10, 25-27, 85-88 and 102-104 are rejected under **35 U.S.C. 103(a)** as being unpatentable over Zaidi, Jim Handy, Taylor, Jeddeloh and Barroso as applied to claims 1, 6, 11, 13-14, 16-17, 44-48 and 79-84 above, and further in view of Alexander et al. (6,131,155).

As per claims 7-8, Zaidi, Jim Handy, Taylor, Jeddeloh and Barroso teach all the limitations of claims 1-6 above but fail to teach direct interfaces from CPUs to memory devices. Alexander teaches CPU programmed to accessing main memory directly, bypassing cache access (Alexander, abstract).

It would have been obvious to one having ordinary skill in the art at the time of the invention to utilize the direct access interface to memory, bypassing the cache as

taught by Alexander in the system of Zaidi, Jim Handy, Taylor, Jeddeloh and Barroso, because data caches provides performance improvement only if program execution performs repeated accesses of data over a short period of time to a small group of data and large amounts of data transfers degrades the performance, so bypassing a cache and directly reading data from memory increases the performance (Alexander, abstract, col. 2, lines 21-56). Also providing a direct and independent interface avoids bus or memory bank conflict as explained with respect to claims 1 and 6 above.

As per claim 9, Zaidi and Barroso teach an arbiter and MAC (Zaidi, fig. 2, items 242, 244) and switch (Barroso, fig.1, item 120) to resolve memory access conflict (Zaidi, column 23, lines 40-45) but fail to teach arbiter for direct read/write interface. It would have been obvious to one having ordinary skill in the art at the time of the invention would provide arbiter for direct (bypassing cache interface) interface, because when multiple CPUs accessing memory device providing arbitration avoids the conflict for same data.

As per claim 10, Zaidi teach an application specific integrated circuit (ASIC) which can be used to provide interconnection structure and method for efficient integration variety functional circuits (Zaidi, column 2, lines 63-65). It would have been obvious to one having ordinary skill in the art at the time of invention have used the embedded system of Zaidi to control the hard disk drive and its components for better performance and compact design.

Claims 25-27, 85-88 and 102-104 are rejected under same rationale as applied to claims 7-10 as above.

6. Claims 19, 58 and 96 are rejected under **35 U.S.C. 103(a)** as being unpatentable over Zaidi, Jim Hardy, Taylor, Jeddeloh and Barroso and further in view of Veidenbaum et al. (Adapting Cache Line Size to Application Behavior, pub. 1999).

Claims 19, 58 and 96 are similar in scope with combination of claims 1-6 above. But the combination of Zaidi, Jim, Taylor, Jeddeloh and Barroso fail to teach selecting size of the cache line based on application running. Veidenbaum teaches adapting cache line size according to application running (Veidenbaum, abstract).

It would have been obvious to one having ordinary skill in the art at the time of the invention to use cache line size based on application running as taught by Veidenbaum in the system of Zaidi, Jim, Taylor, Jeddeloh and Barroso to improve miss rate and memory traffic (Veidenbaum, abstract).

7. Claims 12, 51 and 90 are rejected under **35 U.S.C. 103(a)** as being unpatentable over Zaidi, Jim Hardy, Taylor, Jeddeloh and Barroso and further in view of Ebner et al. (US 6,928,525).

Claim 12 is similar in scope with combination of claims 1-6 and Zaidi, Jim Hardy, Taylor, Jeddeloh and Barroso teach all the limitations, but they combined failed to teach accessing one page by one of first and second CPUs, while other of first and second CPUs is accessing another page. Ebner teaches shared cache memory, which allows multiple simultaneous accesses to data held in different cache lines of cache (Ebner,

Abstract). It would have been obvious to one having ordinary skill in the art at the time of the invention to utilize shared cache allowing multiple simultaneous access to different lines of cache as taught by Ebner in the system of Zaidi, Jim Hardy, Taylor, Jeddeloh and Barroso to improve system performance by allowing concurrent accesses to cache lines (Ebner, col. 2, lines 32-39).

Claims 51 and 90 are also rejected under same rationales as applied to claim 12.

(10) Response to Argument

Appellant's arguments have been fully considered with the Examiners response set forth below. Appellant mainly argues that Zaidi or any other cited prior art reference fails to teach or suggest **switch including plurality of selectors** that each receive second address and **each select between first and second sets of signals relating to first and second memory devices** (appeal brief, page 10).

In response to Appellant's argument, Examiner would like to point out that Zaidi teaches a system (Zaidi, fig. 1, item 100) with a processor (Zaidi, fig. 1, item 110), a cache (fig. 1, item 126) and two memories (fig. 1, item 106 flash memory and item 108 SDRAM memory) accessed through MAC (memory access controller, fig. 1, item 140). Here it is readily apparent (and very well known in the art) that when processor issues memory access request it includes an address of the data residing in the memory and if the system uses virtual memory (see Taylor) than at some point before data from

memory is accessed the virtual (first) address is converted into physical (second)

address. Zaidi further teaches: (see col. 23, lines 22-45) and (col. 24, lines 25-33):

"FIG. 20 represents a standard memory controller. Switched channel memory controller embodiments of the present invention, as illustrated in FIGS. 21 and 22, are possible which allow multiple DMA devices (and processors) to simultaneously communicate with multiple output channels. These output channels can be connected to external memory, internal memory, or non-DMA blocks. As with a standard memory controller, any DMA peripherals and CPUs supply a request and an address to a switched channel memory controller. However, the address includes both the port, device or memory bank address, and the requested memory location address. Once a requested port, device or bank is free, the requesting DMA or CPU is granted access and can begin transferring data. While data transfer is in progress on the requested port, another DMA peripheral or CPU can simultaneously transfer data to a different port for almost limitless bandwidth, while requiring minimal changes to the rest of the system.

A switched channel memory controller can be configured to allow particular DMAs or CPUs to-access only certain channels. For example, a CPU instruction bus can be connected to an external flash memory through one channel, or an external SDRAM memory through another channel"

"**A switch allows execution by either processor from off-chip flash memory**. Data may be transferred to or from a dual-port RAM by a DMA peripheral, or the CPU for processing by the DSP. Or data may be transferred to or from the SDRAM for CPU processing.

With a switched channel memory controller, the CPU can execute from flash memory while simultaneously processing data from a DMA peripheral in the SDRAM. The DSP can at the same time process data from the dual-port RAM while another peripheral is transferring data to or from the RAM."

From above paragraph it is apparently clear that Zaidi teaches "a switch" (here it is noted that the MAC (or switch) of Zaidi provides the same functionality as of the Appellant's switch, i.e. to connect processor/cache to either a flash memory or an SDRAM), however he explicitly fails to teach, switch having plurality of selectors (e.g. multiplexers) each receiving a second address (e.g. physical address translated from

virtual address) and selecting between the first and second set of signals. However, the Examiner contends signals such as chip select, response, data, address, acknowledgement, clock etc. are inherently required to access particular memory device (i.e. out of multiple memories), if such signals are not applied (or selected) than the system will not perform its functionality as intended. To support the Examiner's assertion, Jeddeloh was introduced as evidential reference. The Appellant contends that the Examiner fail to provide evidence that the switch of Jeddeloh includes plurality of selectors that selects between sets of signal based on the address (appeal brief, page 14). However, the Examiner would like to point out that Jeddeloh teaches: (see fig. 3 and col. 4, lines 9-55):

"The memory hub 130 includes **a processor interface 150 that is coupled to the processor 104 through a plurality of bus and signal lines, as is well known in the art. The processor interface 150 is, in turn, coupled to a switch 160 through a plurality of bus and signal lines**, including a write data bus 154 and a read data bus 156, although a single bi-directional data bus may alternatively be provided to couple data in both directions between the processor interface 150 in the switch 160. The processor interface 150 is also coupled to switch 160 through a request line 164 and a snoop line 168. A snoop signal coupled from the switch 160 to the processor interface 150 through the snoop line 168 is used to maintain cache consistency, as will be described in greater detail below. **A request signal coupled from the processor interface 150 to the switch 160 through the request line 164 provides the switch 160 with information corresponding to a request to transfer data through the switch 160**. It will be understood, however, that the processor interface 150 maybe coupled to the switch 160 with a greater or lesser number of buses and signal lines or buses and signal lines different from those illustrated in FIG. 3.

The **switch 160 is also coupled to three memory interfaces 170a-c which are, in turn, coupled to the system memory devices 140a-c, respectively**. By providing a separate and independent memory interface 170a-c for each system memory device 140a-c, respectively, the memory hub 130 avoids bus or memory bank conflicts that typically occur with single channel memory architectures. The **switch 160 is coupled to each memory interface through a plurality of bus and signal lines**, including a write data bus 174, read data bus 176 and a request line 178. However, it will be understood that a single bi-directional data bus may alternatively be used instead of a

separate write data bus 174 and read data bus 176. Significantly, each memory interface 170a-c is specially adapted to the system memory devices 140a-c to which it is coupled. More specifically, each memory interface 170a-c is specially adapted to provide and receive the specific signals received and generated, respectively, by the system memory device 140a c to which it is coupled. Also, the memory interfaces 170a-c are capable of operating with system memory devices 140a-c operating at different clock frequencies. As a result, the memory interfaces 170a c isolate the processor 104 from changes that may occur at the interface between the memory hub 130 and memory devices 140a-c coupled to the hub 130, and it provides a more controlled environment to which the memory devices 140a-c may interface."

From above explanation, it is entirely clear that Appellant's arguments that Examiner fail to provide prima facie case of inherency of selecting respective set of signals are not persuasive. It also further noted that Zaidi explicitly fails to provide detailed description of switch including plurality of selectors (multiplexers), however Jeddeloh again teaches that such switches are conventional in the art (see col. 4, lines56-65):

"The **switch 160 coupling the processor interface 150 to the memory interfaces 170a-c can be any of a variety of conventional or hereinafter developed switches**. For example, the switch 160 may be a cross-bar switch that can simultaneously couple at the processor interface 150 and the memory interfaces 170a-c to each other. **The switch 160 can also be a set of multiplexers** that do not provide the same level of connectivity as a cross-bar switch but nevertheless can couple the processor interface 150 to each of the memory interfaces 170a-c."

Thus, as per Jeddeloh the conventional switch **including set of multiplexers** (switch with plurality of selectors) is well known in the art and it is examiner's assertion that switch including a plurality of multiplexers must inherently receive plurality of signals (e.g. chip select, response, acknowledgement, data, address and clock) based on address provided by the processor and select respective set of signals to access one of first and second memories (e.g. flash or SDRAM) for data access. It is again noted

that if signals are not applied than the appropriate memory will not be enabled and/or selected and the data accesses will not be performed, as such the Examiner contends selecting respective signals is inherent for proper operation of the system.

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

Kaushik Patel

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Examiner, AU 2188

Conferees:

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Supervisory Patent Examiner, Art Unit 2188

04/23/08

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WQAS, TC2100, WG2180